



Product Brief

There is a Chipset for Dual-Processor Server Platforms that Maximizes System Bus, Memory, and I/O Bandwidth

The Intel® E7501 chipset represents the next step in Intel®-based server chipset technology and combines with the Intel® Xeon™ processor with 533 MHz system bus for greater performance.

Platform Overview

The Intel® E7501 chipset represents the next step in Intel®-based server chipset technology. The second in a family of volume server chipsets, the Intel E7501 chipset supports dual-processor server platforms optimized for the Intel® Xeon™ processor with 533 MHz system bus and Intel® NetBurst™ microarchitecture. The Intel E7501 chipset design delivers maximized system bus, memory, and I/O bandwidth to enhance performance, scalability, and end-user productivity while providing a smooth transition to the next-generation server technologies.

Benefits of Advanced Technology and I/O Flexibility

The Intel E7501 chipset utilizes a modular design and offers platform implementation flexibility to meet the expanding needs of dual-processor (DP) servers through three core components:

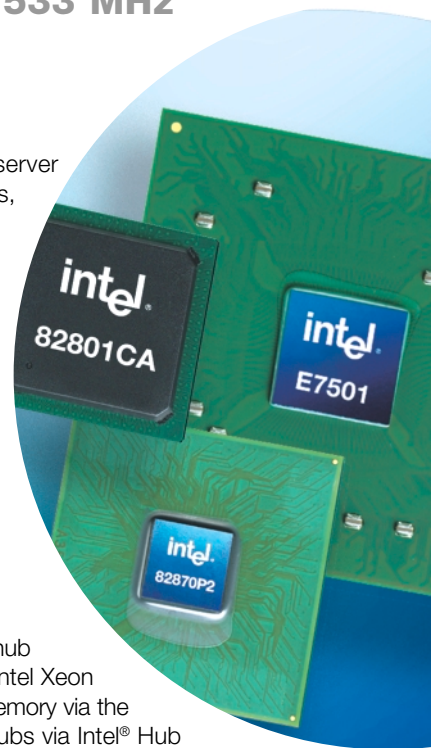
The Intel E7501 Memory Controller Hub (MCH) is the central hub for all data passing through core system elements such as the dual Intel Xeon processor via the system bus interface, the Double Data Rate (DDR) memory via the memory interface, and both the 64-bit PCI/PCI-X and I/O controller hubs via Intel® Hub Interfaces. The Intel E7501 chipset delivers compelling performance at 4.3 GB/s of bandwidth across the 533 MHz system bus and up to 4.3 GB/s of bandwidth across two high-performance DDR SDRAM memory channels. The MCH also allows several high-bandwidth I/O configuration options for a total of 3.2 GB/s of I/O bandwidth. Together, these features deliver high throughput system performance for dual-processor server platforms.

The Intel® 82870P2 64-bit PCI/PCI-X Controller Hub 2 connects to the MCH through a point-to-point Hub Interface 2.0 connection. Up to three Intel 82870P2 Controller Hub devices can be attached to the MCH, each providing bandwidth of over 1.066 GB/s for a total of 3.2 GB/s of I/O bandwidth. Each Intel 82870P2 Controller Hub device contains two independent 64-bit PCI-X interfaces and two PCI hot plug controllers, one per PCI-X interface. Each 64-bit PCI-X segment supports multiple PCI-X slots for high-bandwidth connectivity of next-generation components such as Intel® Gigabit Ethernet adapters and Intel® I/O processors.

The Intel® 82801CA I/O Controller Hub connects to the MCH through a point-to-point Hub Interface 1.5 connection. The Intel 82801CA I/O Controller Hub provides legacy I/O interfaces through integrated features including a two-channel Ultra ATA/100 bus master IDE controller and three USB controllers for up to six USB ports. The Intel 82801CA I/O Controller Hub also offers an integrated System Manageability Bus 2.0 (SMBus 2.0) controller, an integrated LAN controller, as well as AC'97 2.2-compliant and PCI 2.2-compliant interfaces.

Platform Features that Maximize Performance

- Dual Intel Xeon processors with a 533 MHz system bus provide up to 4.3 GB/s of available bandwidth.
- Dual DDR-266 memory channels operate in lock-step to provide up to 4.3 GB/s of memory bandwidth.
- Three Hub Interface 2.0 connections provide multiple high-bandwidth I/O configuration options, yielding up to 3.2 GB/s of I/O bandwidth.



Intel®
E7501 Chipset



Features	Benefits
Supports two Intel® Xeon™ processors with 533 MHz system bus for DP-based server platforms	Delivers a platform that brings Intel® NetBurst™ microarchitecture and the Hyper-Threading Technology of the Intel Xeon processor to deliver world-class performance for peak server workloads.
533 MHz system bus capability	Supports a high-performance platform by enabling a 4.3 GB/s system bus bandwidth that can support greater memory and I/O bandwidths.
Intel® Hub Architecture 2.0 connection to the MCH	This point-to-point connection between the MCH and the three Intel 82870P2 Controller Hub devices provides greater than 1 GB/s of bandwidth. Error Correction Code (ECC) protection, coupled with high data transfer rates, supports I/O segments with greater reliability and faster access to high-speed networks.
Intel® 82870P2 Controller Hub	Introduces next-generation PCI/PCI-X performance and significantly enhances platform flexibility. Two independent 64-bit, 133 MHz PCI-X segments and two hot-plug controllers (one per segment) for each Intel 82870P2 Controller Hub device allow up to six PCI-X buses per system.
Dual-channel DDR-266 memory interface	Offers a maximum memory bandwidth of 4.3 GB/s through a 144-bit wide, 266 MHz Double Data Rate SDRAM memory interface with densities up to 512 megabits.
Advanced Platform RASUM	Features such as memory ECC with Intel® x4 Single Device Data Correction**, hardware memory scrubbing, MCH SMBus target interface, hub interface ECC, and the availability of enhanced error status information maintained through reset yield a more reliable platform.

Products	Package
Intel® E7501 Memory Controller Hub (MCH)	1005 Flip Chip-Ball Grid Array (FC-BGA)
Intel® 82801CA Integrated Controller Hub	421 Ball Grid Array (BGA)
Intel® 82870P2 64-bit PCI/PCI-X Controller	567 Flip Chip-Ball Grid Array (FC-BGA)

Intel Access	
Products Web Site	http://www.intel.com/products/server
Intel® Chipsets Home Page	http://www.intel.com/products/server/chipsets
Intel® Xeon™ Processor with 533 MHz system bus	http://www.intel.com/design/xeon
Intel® Gigabit Ethernet Controllers	http://developer.intel.com/design/network/products/ethernet/index.htm
Intel® I/O Processor	http://developer.intel.com/design/iao/index.htm
Other Intel Support: Intel Literature Center	http://developer.intel.com/design/litcentr (800) 548-4725 7 am - 7 pm CST (USA and Canada) International locations please contact your local sales office.
General Information Hotline	(800) 628-8686 or (916) 356-3104 5 am - 5 pm PST

For more information, visit the Intel® Web site at:
<http://developer.intel.com>

UNITED STATES AND CANADA

Intel Corporation
Robert Noyce Bldg.
2200 Mission College Blvd.
P.O. Box 58119
Santa Clara, CA 95052-8119
USA

EUROPE

Intel Corporation (UK) Ltd.
Pipers Way
Swindon
Wiltshire SN3 1RJ
UK

ASIA-PACIFIC

Intel Semiconductor Ltd.
32/F Two Pacific Place
88 Queensway, Central
Hong Kong, SAR

JAPAN

Intel Japan (Tsukuba HQ)
5-6
Tokodai Tsukuba-shi
300-2635 Ibaraki-ken
Japan

SOUTH AMERICA

Intel Semicondutores do Brasil LTDA
Av. Dr. Chucuri Zaidan, 940-10º andar
04583-904 São Paulo, SP
Brazil

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**In a x4 DDR memory device, the Intel® x4 Single Device Data Correction (x4 SDDC), provides error detection and correction for 1, 2, 3, or 4 data bits within that single device and provides error detection, up to 8 data bits, within two devices.

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